

Fig. 1

Fig. 2

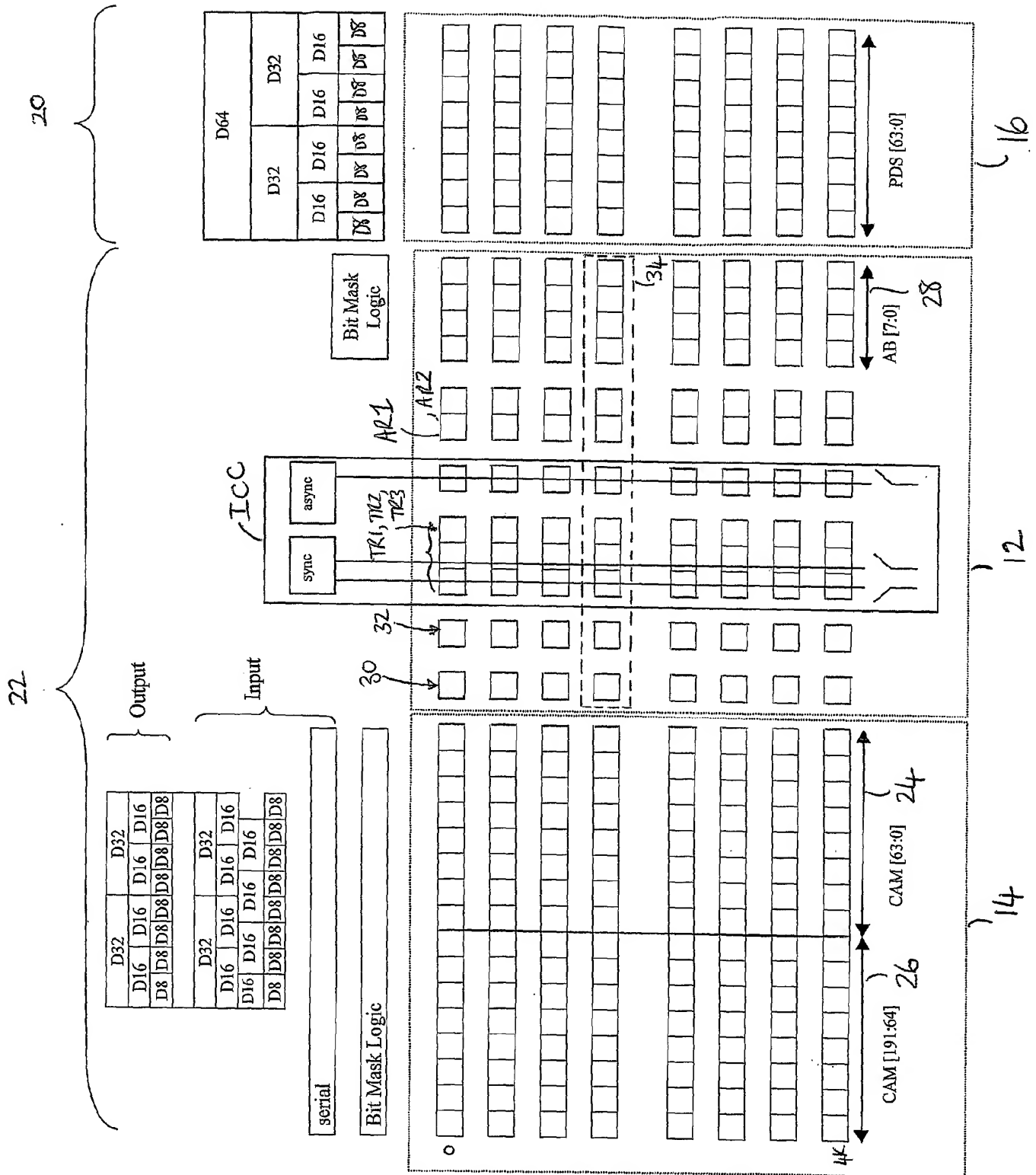
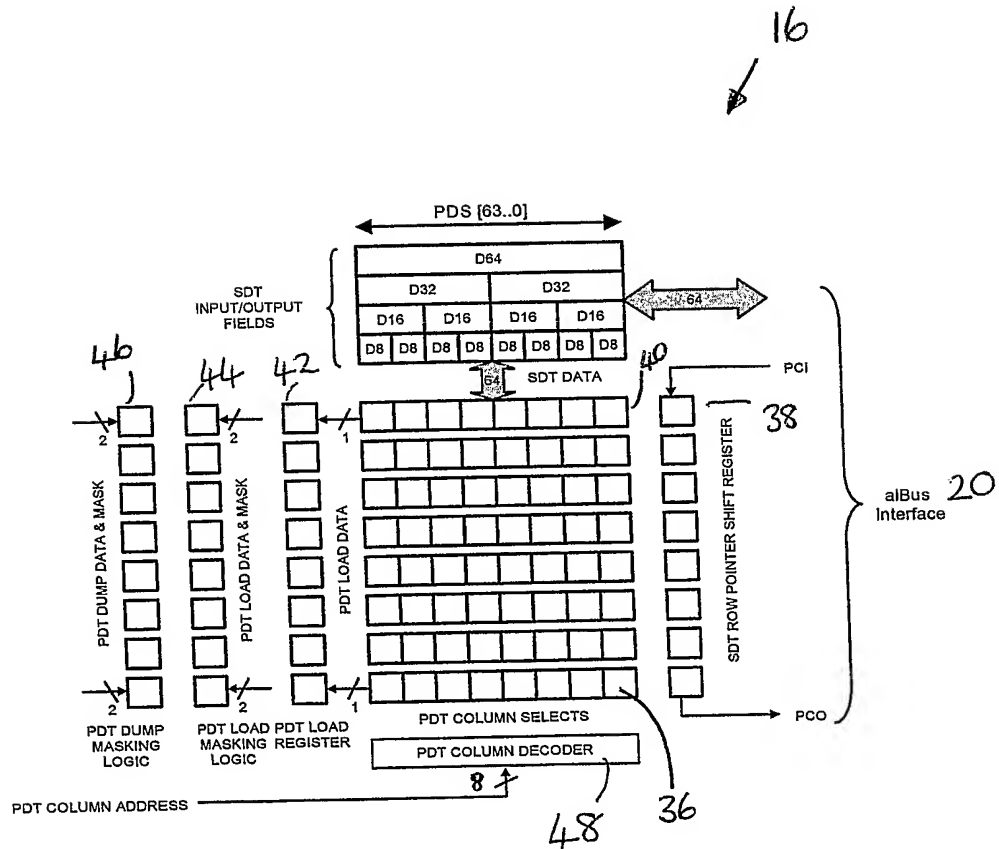


Fig. 3



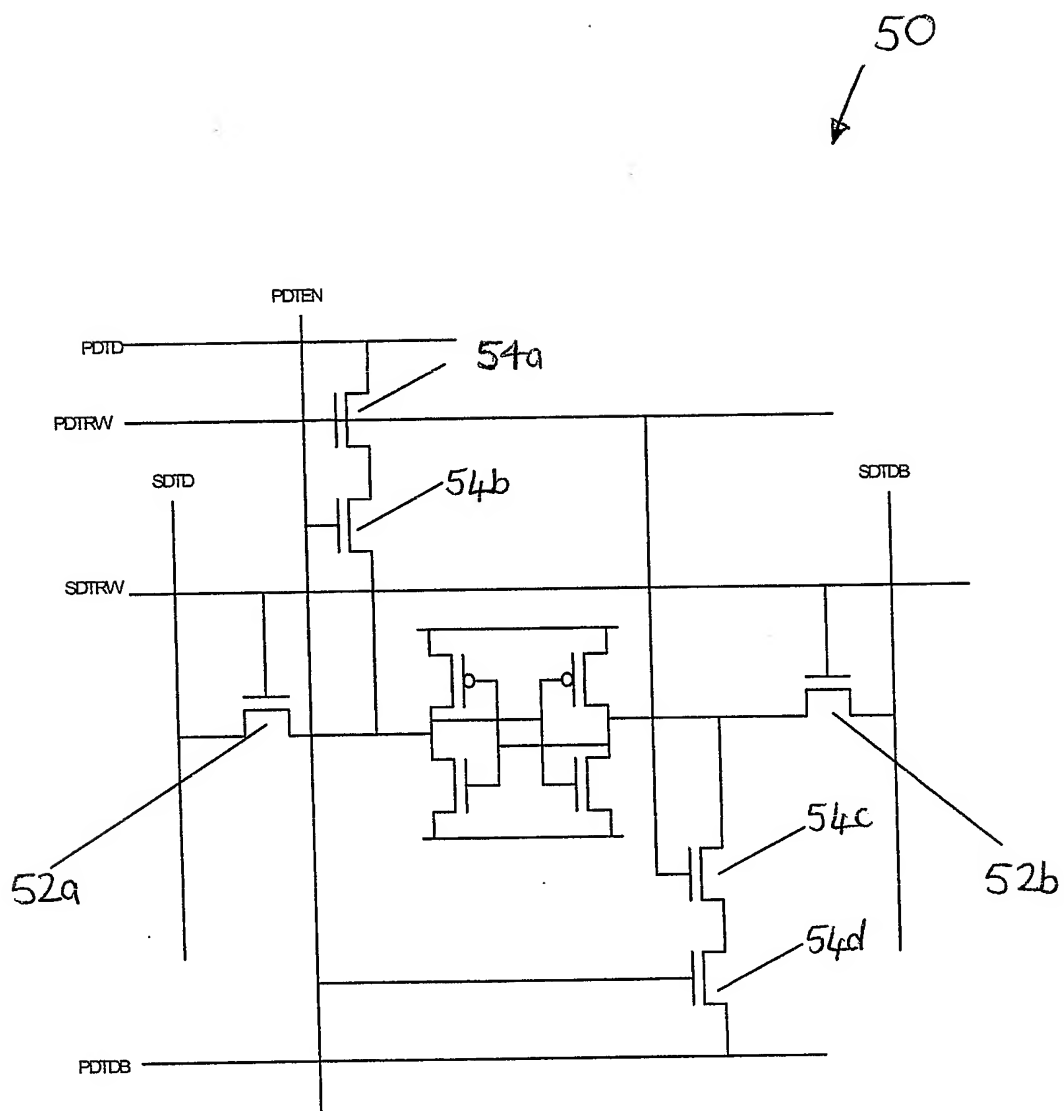


Fig. 4

row address MOD 8	Row Strobe logic conditions
0	$SDTRW\_A[0] = RS[0]$
	$SDTRW\_B[0] = \sim D8.RS[0]$
	$SDTRW\_C[0] = (D32+D64).RS[0]$
	$SDTRW\_D[0] = D64.RS[0]$
1	$SDTRW\_A[1] = (D8+D64).RS[1]$
	$SDTRW\_B[1] = (D16+D64).RS[1]$
	$SDTRW\_C[1] = (D32+D64).RS[1]$
	$SDTRW\_D[1] = D64.RS[1]$
2	$SDTRW\_A[2] = \sim D16.RS[2]$
	$SDTRW\_B[2] = (D16+D64).RS[2]$
	$SDTRW\_C[2] = (D32+D64).RS[2]$
	$SDTRW\_D[2] = D64.RS[2]$
3	$SDTRW\_A[3] = (D8+D64).RS[3]$
	$SDTRW\_B[3] = \sim D8.RS[3]$
	$SDTRW\_C[3] = (D32+D64).RS[3]$
	$SDTRW\_D[3] = D64.RS[3]$
4	$SDTRW\_A[4] = (D8+D64).RS[4]$
	$SDTRW\_B[4] = \sim D8.RS[4]$
	$SDTRW\_C[4] = (D32+D64).RS[4]$
	$SDTRW\_D[4] = D64.RS[4]$
5	$SDTRW\_A[5] = \sim D16.RS[5]$
	$SDTRW\_B[5] = (D16+D64).RS[5]$
	$SDTRW\_C[5] = (D32+D64).RS[5]$
	$SDTRW\_D[5] = D64.RS[5]$
6	$SDTRW\_A[6] = (D8+D64).RS[6]$
	$SDTRW\_B[6] = (D16+D64).RS[6]$
	$SDTRW\_C[6] = (D32+D64).RS[6]$
	$SDTRW\_D[6] = D64.RS[6]$
7	$SDTRW\_A[7] = RS[7]$
	$SDTRW\_B[7] = \sim D8.RS[7]$
	$SDTRW\_C[7] = (D32+D64).RS[7]$
	$SDTRW\_D[7] = D64.RS[7]$

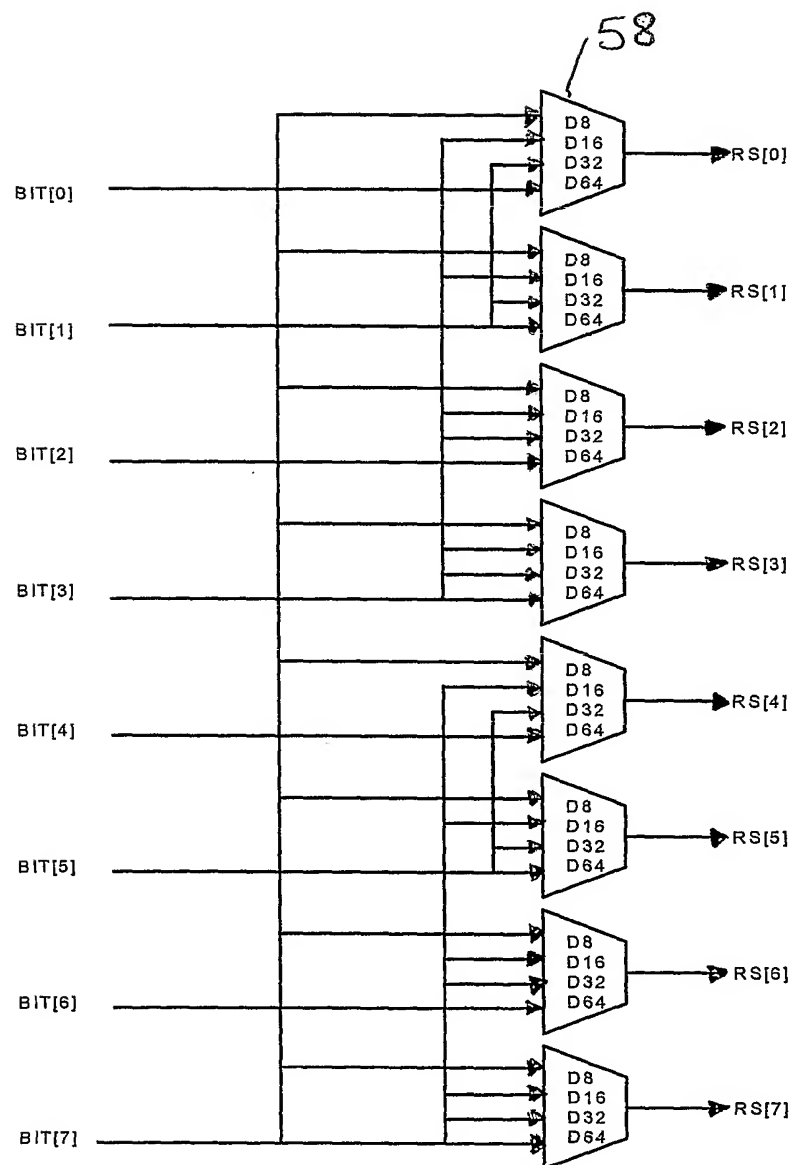
Table 2

Fig. 5

Fig.6

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SDT ROW POINTER SHIFT REGISTER



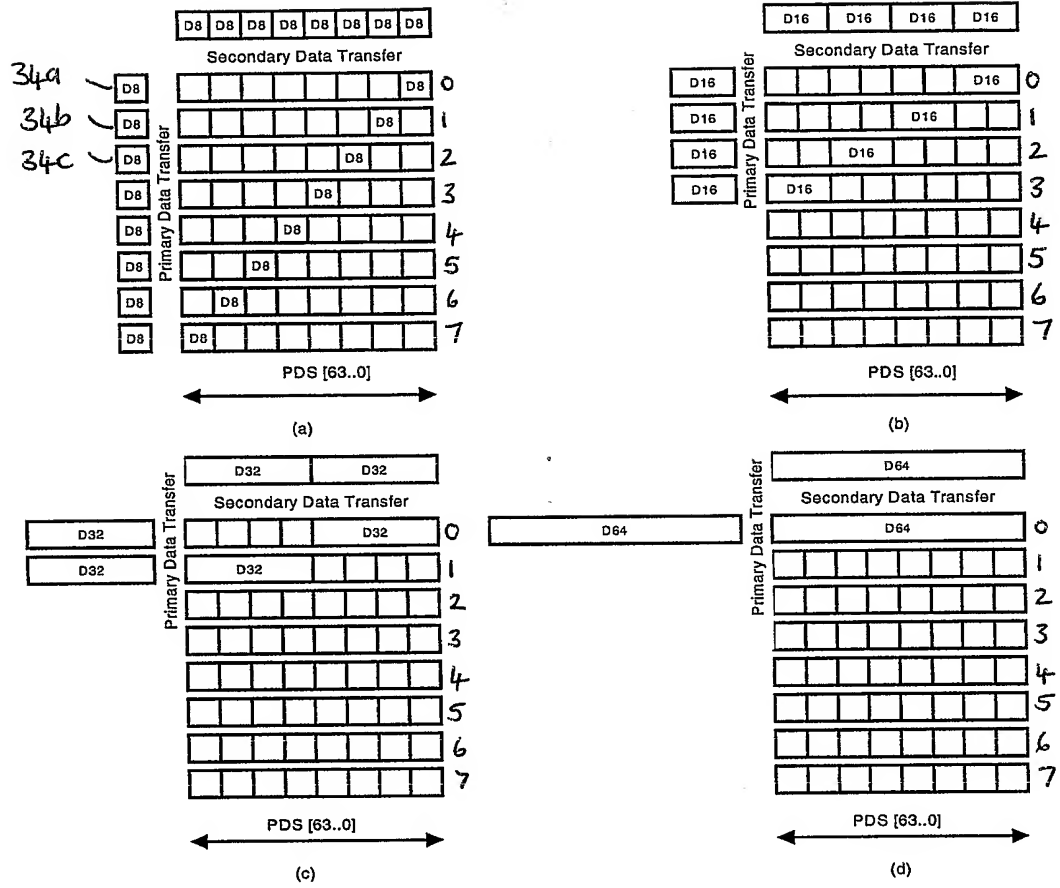


Fig. 7

byte address	column address	Row Strobe logic conditions
0	7..0	PDTEN_A[7..0] = BS[0].CS[7..0]
		PDTEN_B[7..0] = ~D8. BS[0].CS[7..0]
		PDTEN_C[7..0] = (D32+D64). BS[0].CS[7..0]
		PDTEN_D[7..0] = D64. BS[0].CS[7..0]
1	15..8	PDTEN_A[15..8] = (D8+D64). BS[1].CS[15..8]
		PDTEN_B[15..8] = ~D8. BS[1].CS[15..8]
		PDTEN_C[15..8] = (D32+D64). BS[1].CS[15..8]
		PDTEN_D[15..8] = D64. BS[1].CS[15..8]
2	24..16	PDTEN_A[24..16] = ~D16. BS[2].CS [24..16]
		PDTEN_B[24..16] = (D16+D64). BS[2].CS [24..16]
		PDTEN_C[24..16] = (D32+D64). BS[2].CS [24..16]
		PDTEN_D[24..16] = D64. BS[2].CS [24..16]
3	31..25	PDTEN_A[31..25] = (D8+D64). BS[3].CS [31..25]
		PDTEN_B[31..25] = ~D8. BS[3].CS [31..25]
		PDTEN_C[31..25] = (D32+D64). BS[3].CS [31..25]
		PDTEN_D[31..25] = D64. BS[3].CS [31..25]
4	39..32	PDTEN_A[31..25] = (D8+D64). BS[4].CS [39..32]
		PDTEN_B[31..25] = ~D8. BS[3].CS [39..32]
		PDTEN_C[31..25] = (D32+D64). BS[4].CS [39..32]
		PDTEN_D[31..25] = D64. BS[4].CS [39..32]
5	47..40	PDTEN_A[24..16] = ~D16. BS[5].CS [47..40]
		PDTEN_B[24..16] = (D16+D64). BS[5].CS [47..40]
		PDTEN_C[24..16] = (D32+D64). BS[5].CS [47..40]
		PDTEN_D[24..16] = D64. BS[5].CS [47..40]
6	55..48	PDTEN_A[15..8] = (D8+D64). BS[6].CS[55..48]
		PDTEN_B[15..8] = ~D8. BS[6].CS[55..48]
		PDTEN_C[15..8] = (D32+D64). BS[6].CS[55..48]
		PDTEN_D[15..8] = D64. BS[6].CS[55..48]
7	63..56	PDTEN_A[7..0] = BS[7].CS[63..56]
		PDTEN_B[7..0] = ~D8. BS[7].CS[63..56]
		PDTEN_C[7..0] = (D32+D64). BS[7].CS[63..56]
		PDTEN_D[7..0] = D64. BS[7].CS[63..56]

Table 4

Fig. 8



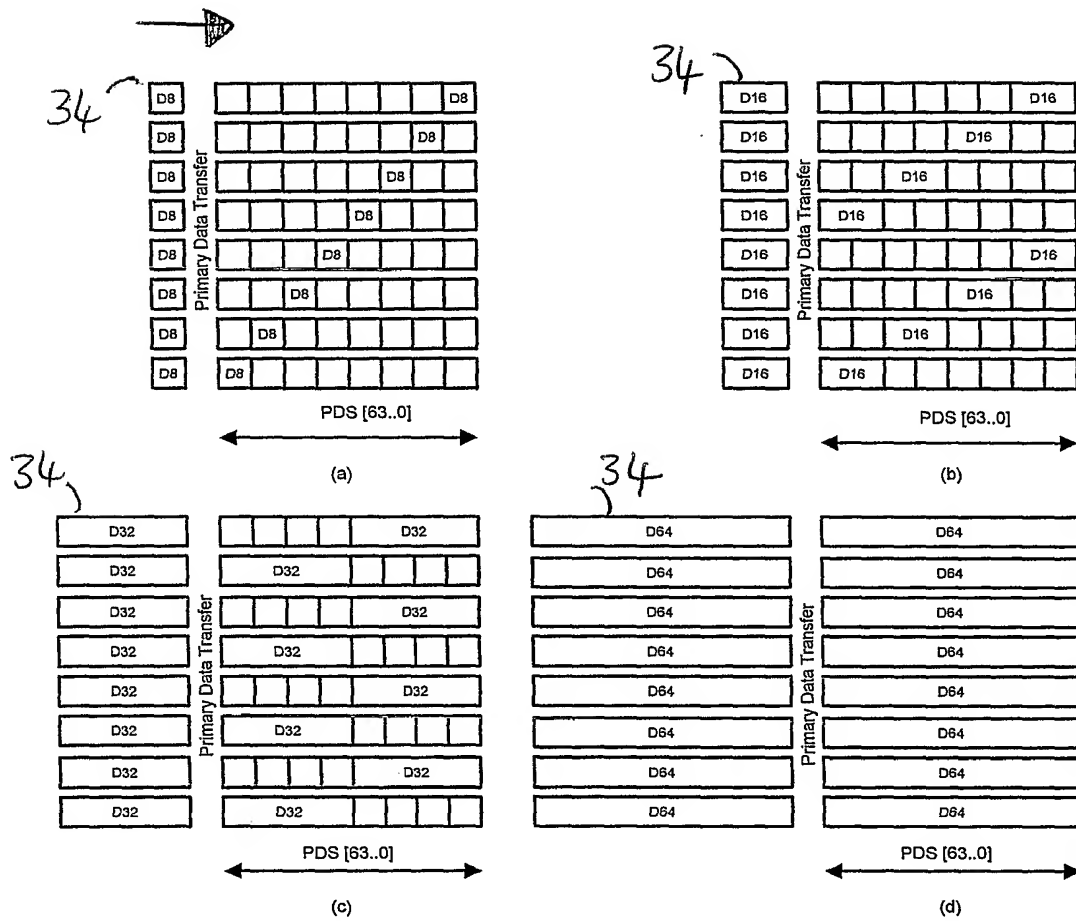


Fig. 9